UNITED STATES PATENT AND TRADEMARK OFFICE

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10/790,986	03/02/2004	Takeo Eguchi	09792909-5828	1289

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 November 2008*.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 9-20* is/are pending in the application.

   4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 9-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

   Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

   Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

   * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO/SB/08)
   Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
   Paper No(s)/Mail Date. _____ .
5)☐ Notice of Informal Patent Application
6)☐ Other: _____.

DETAILED ACTION

1.   This communication is responsive to Amendment filed 11/03/2008.

2.   Claims 1-4 and 9-20 are pending in this application. Claims 1, 9 and 13 are independent

claims.   In Amendment, claims 5-8 are cancelled. This Office Action is made final.

Claim Rejections - 35 USC § 103

3.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

4.   Claims 1-4, 9-13 and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable

over Agrawal et al. (U.S. 4,272,648) in view of Denk et al. (U.S. 2001/0025292 A1).

            Re claim 1, Agrawal et al. disclose in Figures 1-5 a signal processing apparatus

(e.g. Figure 1) for receiving digital signals that are continuously related and input

sequentially (e.g. after sampling and digitized by components 19 and 23 in Figure 1),

performing a predetermined operation on each of sequentially input digital signals (e.g.

Figures 3-5 as typical operations), and outputting a result of the operation (e.g. output of

Figures 3-5 to the next operation), the signal processing apparatus (e.g. Figure 1)

comprising: operation means for performing the predetermined operation on an input

digital signal (e.g. multiplication process as seen in Figure 3 prior reducing word length);

high-order part extraction means for extracting a necessary high-order part by rounding

off a result of the operation performed by the operation means (e.g. component 63 in

Figure 3); difference calculation means for calculating the difference between the result

of the operation performed by the operation means and the high-order part extracted by

the high-order part extraction means (e.g. component 64 in Figure 3); and feedback

means for adding, to a next input digital signal, the difference value calculated by the

difference calculation means or a value obtained by performing a predetermined

operation on the difference value calculated by the difference calculation means (e.g.

feedback as seen in Figure 3 wherein the error is feedback to the adder 62 through delay

element 65 to the next sample).

Agrawal et al. fail to disclose the rounding off means rounding a value to a digit

of an order which is higher than the lowest order digit of the value. However, Denk et al.

disclose in Figures 1-17 the rounding off means rounding a value to a digit of an order

which is higher than the lowest order digit of the value (e.g. component 840 in Figure 8

and paragraphs [0035-0040]).

Therefore, it would have been obvious to a person having ordinary skill in the art

at the time the invention is made to add the rounding off means rounding a value to a

digit of an order which is higher than the lowest order digit of the value as seen in Denk

et al.'s invention into Agrawal et al.'s invention because it would enable to minimize or

eliminate error in reducing wordlength (e.g. paragraph [0009]).

Re claim 2, Agrawal et al. further disclose in Figures 1-5 a second set of

continuously-related digital signals is sequentially input after completion of inputting of a

first set of continuously-related digital signals (e.g. next sample is fed continuously into

the system), a difference value obtained as a result of the difference calculation

performed (e.g. error signal obtained by adder 64), by the difference calculation means,

on the last digital signal of the first set of digital signals or a value obtained by

performing the predetermined operation on the difference value calculated by the

difference means is reset to 0 or added with a particular value (e.g. most significant

digital of error is either 0 or error signal from adder 64 in Figure 3), and the resultant

value is added, via the feedback means, to the first digital signal of the second digital

signals (e.g. by adder 62 in Figure 3).

Re claim 3, Agrawal et al. further disclose in Figures 1-5 feedback means adds, to

the next input digital signal, a value obtained by multiplying the difference value

calculated by the difference calculation means by a factor smaller than 1 (e.g. only the

most significant digit of error signal $e(N)$, technically the error signal is scaled down by

N-1 digits as seen in Figure 3).

Re claim 4, Agrawal et al. further disclose in Figures 1-5 a digital signal acquired

by means of over sampling is input to the operation means (e.g. Figure 5).

Re claim 9, it is a medium claim of claim 1. Thus, claim 9 is also rejected under

the same rationale as cited in the rejection of rejected claim 1.

Re claim 10, it is a medium claim having similar limitations cited in claim 2.

Thus, claim 10 is also rejected under the same rationale as cited in the rejection of

rejected claim 2.

Re claim 11, it is a medium claim having similar limitations cited in claim 3. Thus, claim 11 is also rejected under the same rationale as cited in the rejection of rejected claim 3.

Re claim 12, it is a medium claim having similar limitations cited in claim 4. Thus, claim 12 is also rejected under the same rationale as cited in the rejection of rejected claim 4.

Re claim 13, it is a method claim having similar limitations cited in claim 1. Thus, claim 13 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 17, Agrawal et al. fail to disclose in Figures 1-5 the rounding off a result of the operation performed by the operation means consists of rounding off if a rounded resultant is lower than a predetermined figure. However, Denk et al. disclose in Figures 1-17 the rounding off a result of the operation performed by the operation means consists of rounding off if a rounded resultant is lower than a predetermined figure (e.g. Figure 9).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the rounding off a result of the operation performed by the operation means consists of rounding off if a rounded resultant is lower than a predetermined figure as seen in Denk et al.'s invention into Agrawal et al.'s invention because it would enable to minimize or eliminate error in reducing wordlength (e.g. paragraph [0009]).

Re claims 18-20, Agrawal et al. fail to disclose in Figures 1-5 an error is produced during the rounding off and the error is capable of being input to one of the high-order

part extraction means and a low-order part extraction means depending on a factor; if an

error is equal to or greater than a factor, then the error is input to the high-order part

extraction means, and if the error is less than the factor, then the error is input to a low-

order part extraction means; and an error is produced if the result is not rounded up and is

calculated via the difference calculation means and added to a next input digital signal via

the feedback means. However, Denk et al. disclose in Figures 1-17 an error is produced

during the rounding off and the error is capable of being input to one of the high-order

part extraction means and a low-order part extraction means depending on a factor (e.g.

Figure 9 wherein the factor is the threshold and bias factor); if an error is equal to or

greater than a factor, then the error is input to the high-order part extraction means, and if

the error is less than the factor, then the error is input to a low-order part extraction means

(e.g. Figures 7-9 with the condition comparison with threshold value); and an error is

produced if the result is not rounded up and is calculated via the difference calculation

means and added to a next input digital signal via the feedback means (e.g. inherently

exists in Figures 7-9).

Therefore, it would have been obvious to a person having ordinary skill in the art

at the time the invention is made to add an error is produced during the rounding off and

the error is capable of being input to one of the high-order part extraction means and a

low-order part extraction means depending on a factor; if an error is equal to or greater

than a factor, then the error is input to the high-order part extraction means, and if the

error is less than the factor, then the error is input to a low-order part extraction means;

and an error is produced if the result is not rounded up and is calculated via the difference

calculation means and added to a next input digital signal via the feedback means as seen

in Denk et al.'s invention into Agrawal et al.'s invention because it would enable to

minimize or eliminate error in reducing wordlength (e.g. paragraph [0009]).

5.   Claims 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agrawal et

al. (U.S. 4,272,648) in view of Denk et al. (U.S. 2001/0025292 A1), as applied to claim 1

above, and in further view of the admitted prior art.

Re claims 14-15, Agrawal et al. fail to disclose low-order part extraction means

for extracting a necessary low-order part by rounding off the result of the operation

performed by the operation means; wherein the rounding off means rounding a value to a

digit of an order which is higher than the lowest order digit of the value as if a lower-

order value output from the lower-order part extraction means is equal to or greater than a

predetermined factor, the lower-order value is rounded up to a high-order value and

added to an output of the high-order part extraction means. However, Denk et al.

disclose in Figures 1-17 the rounding off means rounding a value to a digit of an order

which is higher than the lowest order digit of the value (e.g. component 840 in Figure 8

and paragraphs [0035-0040]). Further, the admitted prior art discloses low-order part

extraction means for extracting a necessary low-order part by rounding off the result of

the operation performed by the operation means as if a lower-order value output from the

lower-order part extraction means is equal to or greater than a predetermined factor, the

lower-order value is rounded up to a high-order value and added to an output of the high-

order part extraction means (e.g. pages 2-3).

Therefore it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add low-order part extraction means for extracting a necessary low-order part by rounding off the result of the operation performed by the operation means; wherein the rounding off means rounding a value to a digit of an order which is higher than the lowest order digit of the value as if a lower-order value output from the lower-order part extraction means is equal to or greater than a predetermined factor, the lower-order value is rounded up to a high-order value and added to an output of the high-order part extraction means as seen in Denk et al.'s invention and the admitted prior art into Agrawal et al.'s invention because it would reduce error in average (e.g. page 3 lines 10-13 and paragraph [0009]).

Re claim 16, Agrawal et al. fail to disclose the rounding off a result of the operation performed by the operation means consists of rounding up if a rounded resultant is less than a predetermined figure. However, the admitted prior art discloses the rounding off a result of the operation performed by the operation means consists of rounding up if a rounded resultant is less than a predetermined figure (e.g. pages 2-3).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the rounding off a result of the operation performed by the operation means consists of rounding up if a rounded resultant is less than a predetermined figure as seen in the admitted prior art into Agrawal et al.'s invention because it would enable to reduce error in average (e.g. page 3 lines 10-13).

Response to Arguments

6.   Applicant's arguments filed 11/03/2008 have been fully considered but they are not

persuasive.

     a.   The applicant argues in page 2 for claims rejected under U.S.C. 103(a) that the

cited reference by Agrawal does not disclose the limitation "difference calculation means

for...by the high-order part extraction means" since the Examiner merely discloses or

points to component 64 in Figure 3. In addition, the applicant argues the component 64

in Figure 3 cannot disclose the above limitation since it is just a summer.

        The examiner respectfully submits that the component 64 and its corresponding

        description in the spec logically and reasonably disclose the context of above

        argued limitations wherein adder 64 subtract (e.g. the minus sign on the right

        below the summation sign 64 in Figure 3) the output of component 3 as the high-

        order part extraction from the original operation result of summer 62. Thus, the

        output of adder 64 is the actual difference between the operation result and its

        high-order part extraction from the operation result. Even though, the component

        64 is labeled and drawn as a summer, but it functions as the subtractor for

        computing the differences between the inputs.

     b.   The applicant argues in page 3 first paragraph for claims rejected under 35 U.S.C.

103(a) that the cited reference by Agrawal does not disclose the limitation "feedback

means for adding…by the difference value calculation means".

The examiner respectfully submits that Agrawal does disclose the above argued

limitation in view of the above response, part a, wherein after computing the

difference as addressed above, it feeds the differences back to the original

operation result by the adder 62 for summing the operation result with differences

in Figure 3.

c.   The applicant argues in pages 3-4 last paragraph that the references cannot be

combinable since it would destroying the purpose of Agrawal wherein Agrawals's

purpose is to achieved by discarding part and Denk's purpose is to achieved by rounding.

Thus, discarding and rounding are not analogous and cannot be combined together.

The examiner respectfully submits that neither reference would clearly state that it

would not be combinable with other reference. Based on the technical definition,

discarding and rounding are not completely unanalogous, but rather these two

terms are very similar wherein discarding can be part of the rounding process as

round-off. Rounding can be either round-up as rounding the last bit to the highest

bit; round-down as rounding the last bit to the lowest bit; and round-off is leaving

the last bit unchange, regardless the previous bit. In addition, the whole purpose

of Agrawal et al. is not only discarding the bits, but rather discarding the bits with

minimal error as rounding which is done through the feedback path in Figure 3.

d.   The applicant argues in pages 4-5 that the cited motivation to paragraph [0009] is

improper since it is the invention summary which does not disclose or discuss the

element relied on by the Examiner.

      The examiner respectfully submits that paragraph [0009] discloses the general

concept of the invention rather the specific element or structure of the invention.

As long as the paragraph discloses either inherently or expressively the reasonable

benefits of combining, it would be usable as motivation to combine references. In

addition, there is no requirement to have a specific paragraph states the

motivation with specific elements used for combining with other reference.

e.   The applicant argues in page 5 last two paragraphs for claim 9 that claim 9 is

rejected under the same rationale as claim 1. However, claim 9 is directing to storage

medium which has not addressed in claim 1.

      The examiner respectfully submits that rejection 9 is reasonably stated in the

Office action. As clearly addressed in the action, claim 9 is a medium claim having

similar limitations cited in claim 1. Thus, claim 9 is also rejected under the same

rationale as cited in the rejection of claim 1. Further, storage medium readable is very

common in the computer.

      In addition, in response to applicant's arguments, the recitation in the preamble as

storage medium readable has not been given patentable weight because the recitation

occurs in the preamble. A preamble is generally not accorded any patentable weight

where it merely recites the purpose of a process or the intended use of a structure, and

where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

Conclusion

7.   **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHAT C. DO whose telephone number is (571)272-3721. The examiner can normally be reached on Tue-Fri 9:00AM to 7:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lewis Bullock can be reached on (571) 272-3759. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would

like assistance from a USPTO Customer Service Representative or access to the automated

information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Chat C. Do/
Primary Examiner, Art Unit 2193

November 20, 2008

Application Number	Application/Control No.	Applicant(s)/Patent under Reexamination
	10/790,986	EGUCHI, TAKEO
	Examiner	**Art Unit**
	Chat C. Do	2193